

1 **CLAIMS:**

2 What we claim is:

- 3 1. A data storage device comprising:
4 an array of resistive memory cells having rows and columns;
5 a set of diodes electrically connected in series to a plurality of resistive
6 memory cells in the array;
7 a plurality of word lines extending along the rows of the array;
8 a plurality of bit lines extending along the columns of the array;
9 a first selected resistive memory cell in the array, wherein the first selected
10 resistive memory cell is positioned between a first word line in the plurality of
11 word lines and a first bit line in the plurality of bit lines; and
12 a circuit electrically connected to the array and capable of applying a first
13 voltage to the first word line, a second voltage to the first bit line, and a third
14 voltage to at least one of a second word line in the plurality of word lines and a
15 second bit line in the plurality of bit lines.
16 2. The device of claim 1, wherein the array of resistive memory cells comprises a
17 magnetic random access memory (MRAM) cell.
18 3. The device of claim 2, wherein the MRAM memory cell comprises a tunnel
19 junction.
20 4. The device of claim 1, wherein the set of diodes comprises thin-film diodes.
21 5. The device of claim 1, further comprising a second resistive memory cell in the
22 array, wherein the second resistive memory cell is stacked upon the first selected
23 resistive memory cell.
24 6. The device of claim 1, wherein the circuit is capable of writing to the first selected
25 resistive memory cell by applying sufficient energy to the first word line and the
26 first bit line to transform the first selected resistive memory cell from a first
27 resistance state to a second resistance state.
28 7. The device of claim 1, wherein the circuit is capable of sensing a current flowing
29 through the first selected resistive memory cell.
30 8. The device of claim 1, wherein values of the first voltage and the third voltage are
31 substantially equal.
32 9. The device of claim 1, wherein the circuit is capable of grounding at least one of
33 the second word line and the second bit line.

- 1 10. A method of sensing a resistance state of a first selected resistive memory cell in a
2 data storage device that includes an array of resistive memory cells, a plurality of
3 word lines extending along rows of the array, a plurality of bit lines extending
4 along columns of the array, the first selected resistive memory cell in the array,
5 wherein the first selected resistive memory cell is positioned between a first word
6 line in the plurality of word lines and a first bit line in the plurality of bit lines, and
7 a circuit electrically connected to the array, the method comprising:
8 providing a set of diodes electrically connected to a plurality of resistive
9 memory cells in the array;
10 applying a first voltage to the first word line, a second voltage to the first
11 bit line, and a third voltage to at least one of a second word line in the plurality of
12 word lines and a second bit line in the plurality of bit lines; and
13 sensing a signal current flowing through the first selected resistive memory
14 cell.
15 11. The method of claim 10, further comprising determining a particular resistance
16 state of the first selected resistive memory cell by comparing the signal current to
17 a reference current value.
18 12. The method of claim 10, wherein the providing step comprises providing a set of
19 thin-film diodes.
20 13. The method of claim 10, wherein the sensing step comprises sensing the signal
21 current flowing through a magnetic random access memory (MRAM) cell.
22 14. The method of claim 10, wherein the applying step comprises applying the third
23 voltage to a plurality of word lines other than the first word line.
24 15. The method of claim 10, wherein the applying step comprises applying the third
25 voltage to a plurality of bit lines other than the first bit line.
26 16. The method of claim 10, further comprising sensing a signal current flowing
27 through a second resistive memory cell positioned in a stacked configuration
28 relative to the first selected resistive memory cell.
29 17. The method of claim 10, wherein the applying step comprises applying the first
30 voltage and the third voltage having substantially equal values.
31 18. The method of claim 10, wherein the applying step comprises grounding at least
32 one of the second word line and the second bit line.
33 19. The method of claim 10, further comprising writing data to the first selected
34 resistive memory cell by selecting the first voltage and the second voltage such

- 1 that the first voltage and the second voltage change the first selected memory cell
2 from a first resistance state to a second resistance state.
- 3 20. The method of claim 10, wherein the providing step comprises providing that the
4 set of diodes be electrically connected in series with the plurality of resistive
5 memory cells.